TELTONE®

M-956
DTMF RECEIVER

Description

The Teltone® M-956 (see Figure 1) combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. Fabricated as a monolithic integrated circuit using low-power CMOS processing, the M-956 is packgaged in a 22-pin DIP and operates from a single 5-volt DC supply. An inexpensive 3.58-MHz television crystal and resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

The SIGNAL IN input to the M-956 (see Figure 2) interfaces readily to telephone lines, radio receivers, tape players, and other DTMF signal sources. The input stages of the M-956 filter out noise, split the signal into its high-frequency-group and low-frequency-group components, and hard-limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Post-processing stages of the M-956 time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors, and are three-state enabled to facilitate bus-oriented architectures.

Features

- Complete DTMF receiver in 22-pin DIP (plastic or CerDIP)
- Decodes all 16 DTMF digits
- Excellent speech immunity
- Meets telephone impulse noise immunity standards
- Selectable 4-bit hexadecimal or binary coded 2-of-8 output
- Fabricated using low-power CMOS technology
- Operates on single DC supply
- Uses inexpensive 3.58-MHz crystal
- Three-state outputs

Applications

- Central office products
- PBX and key systems
- Radio telephones
- Remote control and monitoring devices
- Computer data entry systems

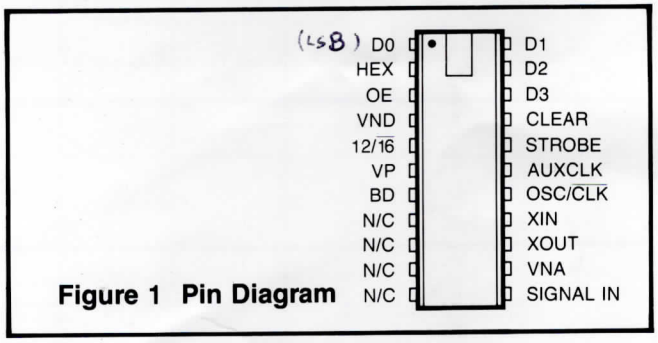

Figure 1 Pin Diagram

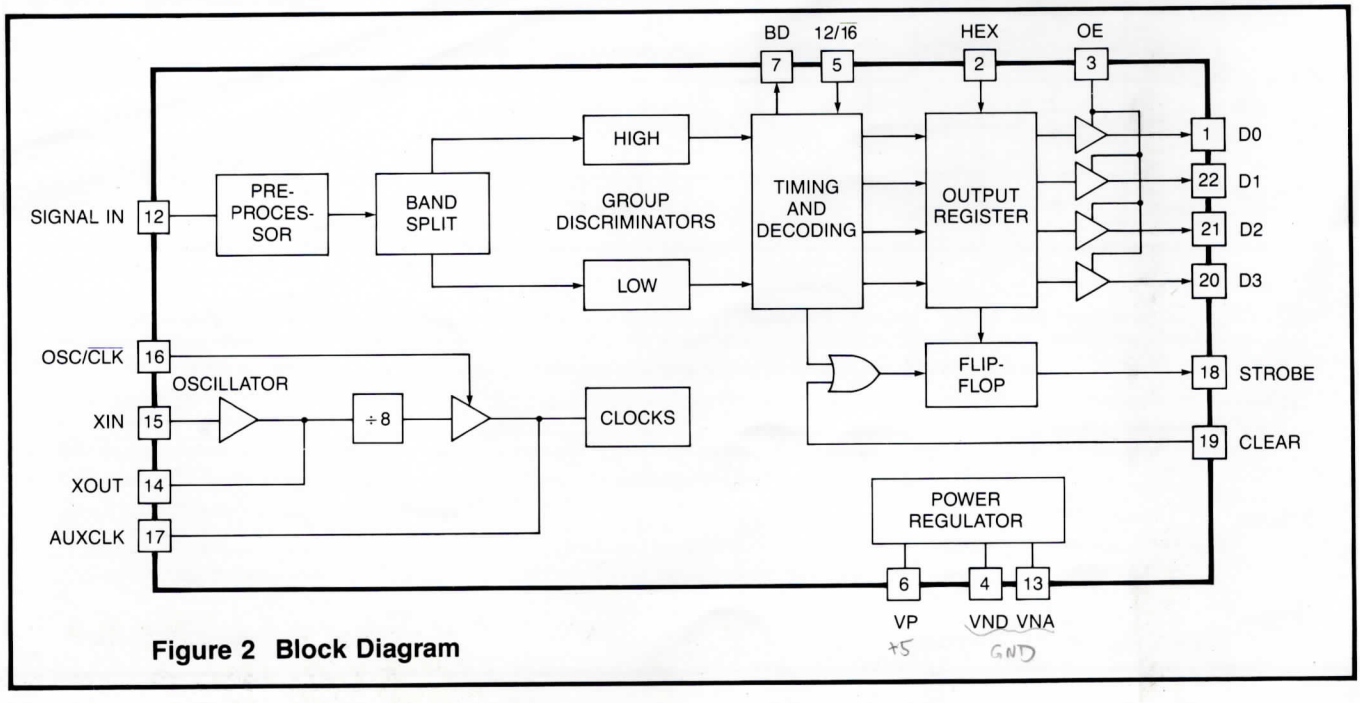

Figure 2 Block Diagram

Table 1 Pin Functions

Pin	Function
SIGNAL IN	DTMF input. Timings are shown in Figure 3. Internally biased so that the input signal may be AC coupled. SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 6. See Table 2 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1", the M-956 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0", the M-956 detects all 16 DTMF signals (1 through D).
D3, D2, D1, D0	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 2. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 3.
OE	Output enable. When OE is at logic "1", the data outputs are in the CMOS push/pull state and represent the contents of the output register (see Figure 2). When OE is driven to logic "0", the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 3.
HEX	Binary output format control. When HEX is at logic "1", the output of the M-956 is full, 4-bit binary. When HEX is at logic "0", the output is binary coded 2-of-8. Table 2 shows the output codes.
STROBE	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1", whichever is earlier. Timings are shown in Figure 3.
CLEAR	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0". When CLEAR is at logic "0", STROBE is forced to logic "0" only when a valid pause is detected.
BD	Early signal presence output. BD indicates that a possible signal has been detected and is being validated. As shown in Figure 3, BD precedes STROBE and the data outputs.
XIN, XOUT	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1". See Figure 6.
OSC/$\overline{CLK}$	Time base control. When OSC/$\overline{CLK}$ is at logic "1", the output of the M-957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the time base.
AUXCLK	Auxiliary clock input. When OSC/$\overline{CLK}$ and XIN are at logic "0", the AUXCLK input is selected as the M-956's time base. The auxiliary input must be 3.58 MHz divided by 8 for the M-956 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	Positive power supply connection.
N/C	Not connected. These pins have no internal connection and may be left floating.

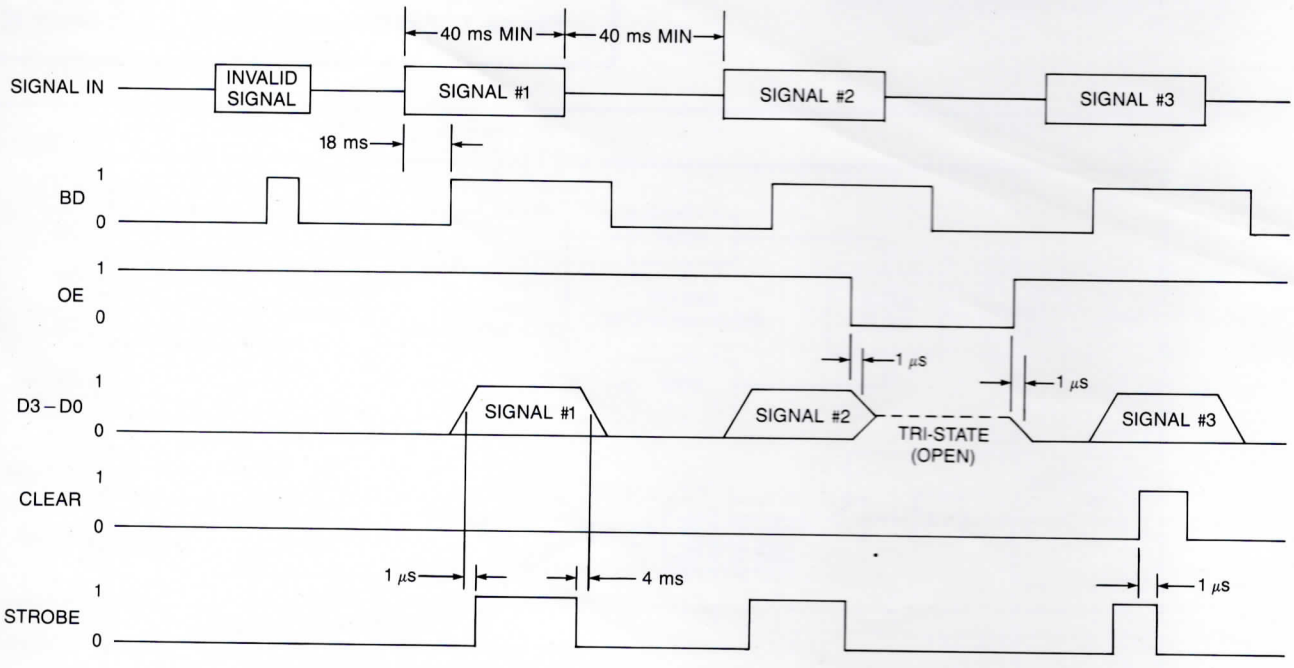

Figure 3 Timing Diagram

Table 2 DTMF to Binary Decoding

SIGNAL	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT FORMAT	2-OF-8 OUTPUT FORMAT
			3 2 1 0	3 2 1 0
1	697	1209	0 0 0 1	0 0 0 0
2	697	1336	0 0 1 0	0 0 0 1
3	697	1477	0 0 1 1	0 0 1 0
4	770	1209	0 1 0 0	0 1 0 0
5	770	1336	0 1 0 1	0 1 0 1
6	770	1477	0 1 1 0	0 1 1 0
7	852	1209	0 1 1 1	1 0 0 0
8	852	1336	1 0 0 0	1 0 0 1
9	852	1477	1 0 0 1	1 0 1 0
0	941	1336	1 0 1 0	1 1 0 1
*	941	1209	1 0 1 1	1 1 0 0
#	941	1477	1 1 0 0	1 1 1 0
A	697	1633	1 1 0 1	0 0 1 1
B	770	1633	1 1 1 0	0 1 1 1
C	852	1633	1 1 1 1	1 0 1 1
D	941	1633	0 0 0 0	1 1 1 1

Note: The M-956 detects signals A through D only when the $12/\overline{16}$ input is at logic "1".

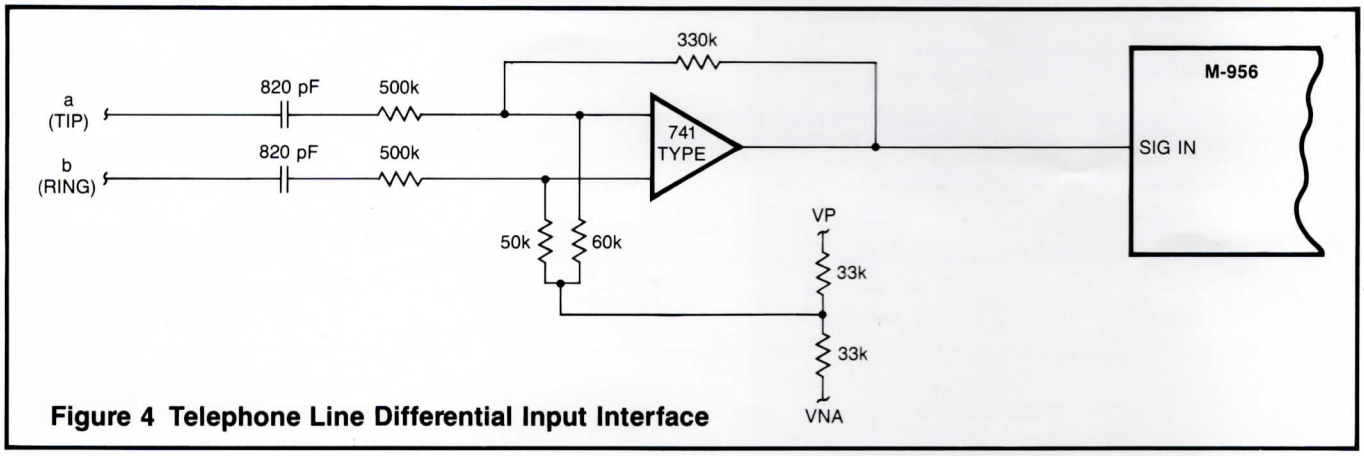

Figure 4 Telephone Line Differential Input Interface

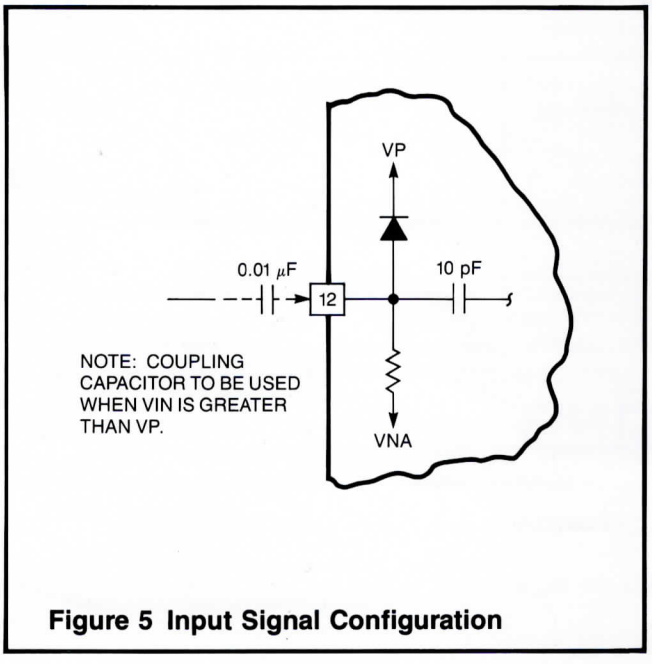

Figure 5 Input Signal Configuration

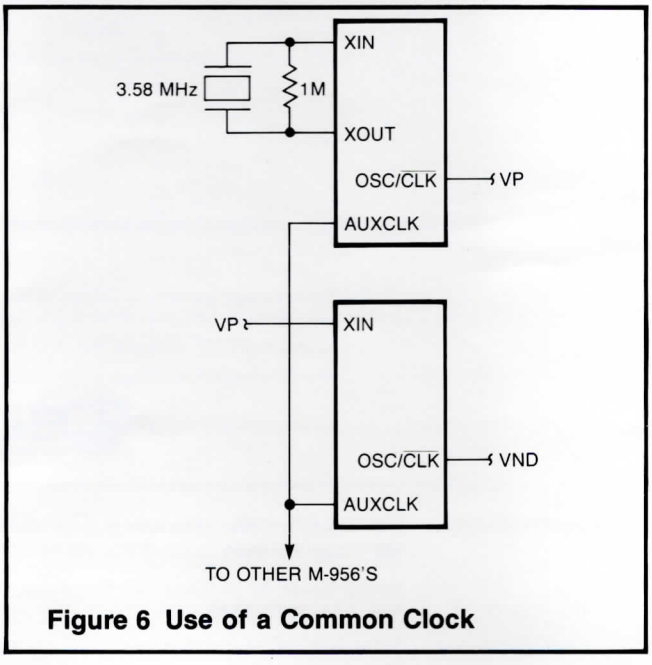

Figure 6 Use of a Common Clock

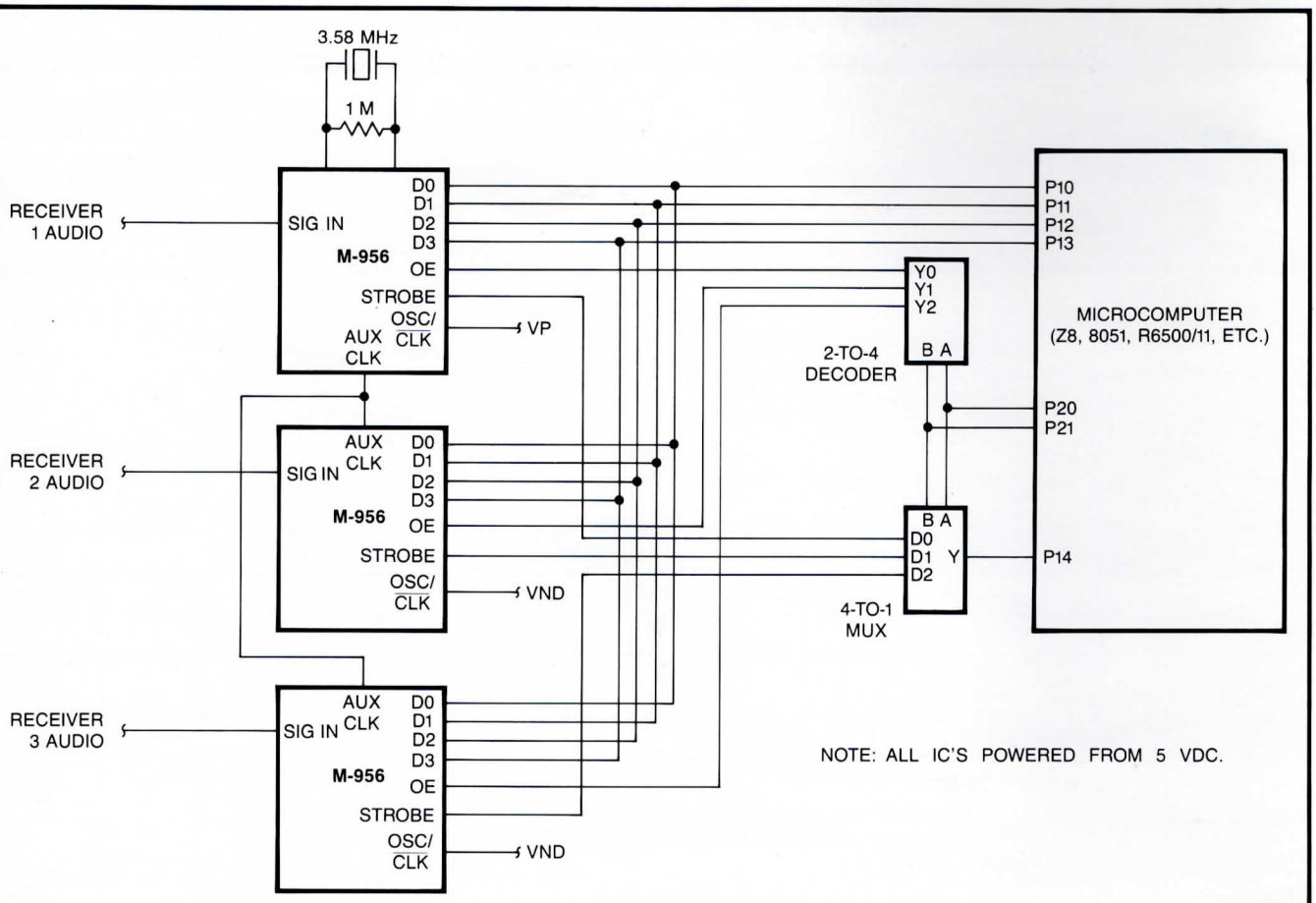

Figure 7 Multiple Receiver/Microprocessor Interface

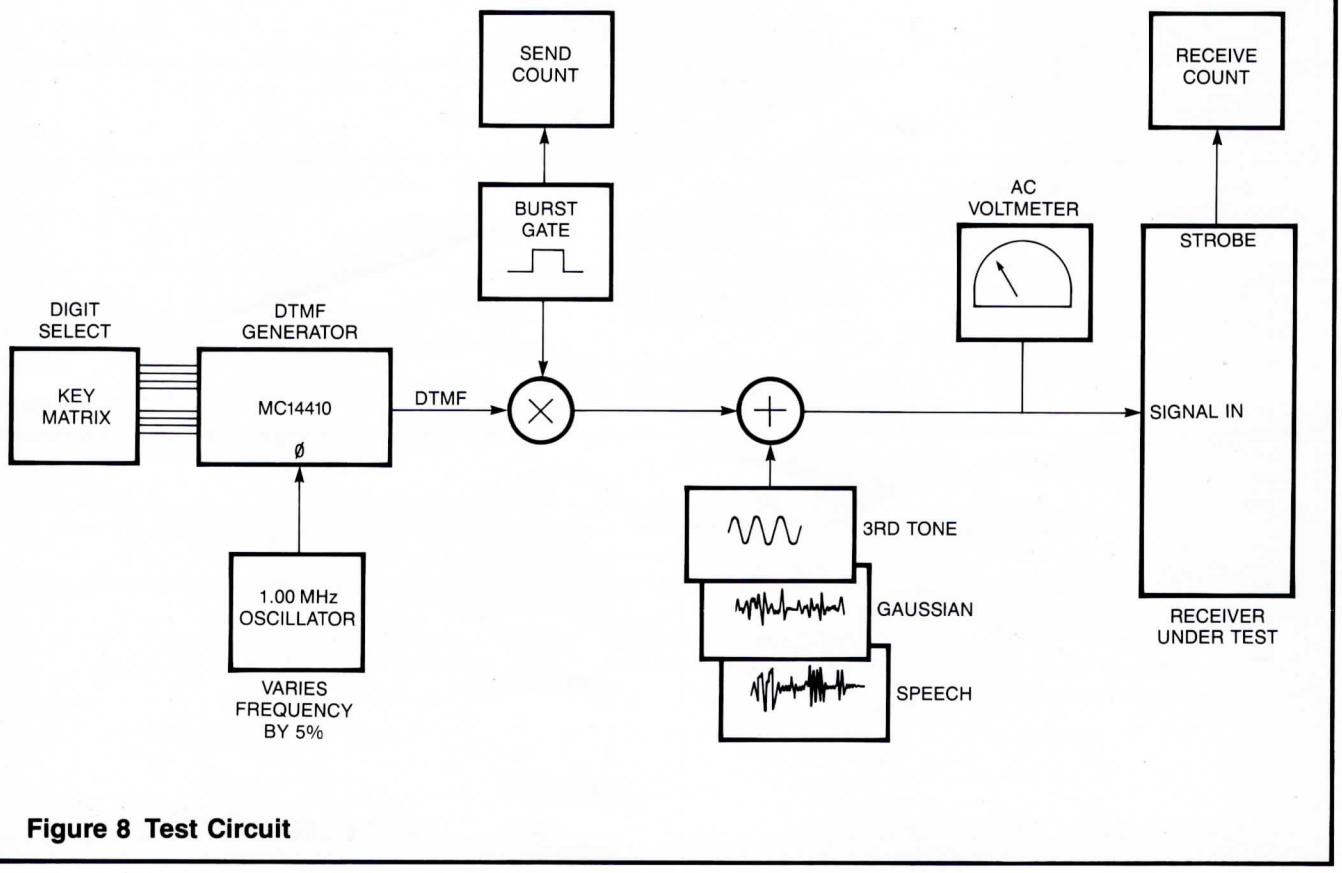

Figure 8 Test Circuit

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2)	7.0 V
Voltage on SIGNAL IN	(VP + 0.5 V) to (VND − 22 V)
Voltage on Any Pin Except SIGNAL IN	(VP + 0.5 V) to (VND − 0.5 V)
Storage Temperature Range	−40° to 85° C
Operating Temperature Range	0° to 70° C
Lead Soldering Temperature	260° C for 5 seconds

Notes:

1. Exceeding these ratings may permanently damage the M-956.
2. VP referenced to VND. VND should be at equal potential to VNA. VND/VNA may be at ground.

Table 4 Specifications

Parameter		Conditions	Min	Typ	Max	Units	Notes
SIGNAL IN Input Requirements	Signal Level (per tone)	—	−27	—	0	dBm	1
	Signal Duration	—	40	30	—	ms	
	Interval Between Signals	—	40	35	—	ms	
	Signal Present Without Detection	—	—	—	20	ms	
	Interruption of Signal Without Redetection	—	—	—	20	ms	
	Signal Frequency Deviation With Detection	—	—	±2.5%	±(1.5% + 2)	Hz	
	Signal Frequency Deviation Without Detection	—	±3.5%	±3.0%	—	Hz	
	Twist	—	—	—	±10	dB	2
	Gaussian Noise	—	—	12	A − 7	dB	3
	Dial Tone Level (per tone, F ≤ 480 Hz)	—	—	—	A + 0	dB	4
Digital Input Requirements	Logic 0 Voltage	—	0	—	1.5	V	5
	Logic 1 Voltage	—	3.5	—	5.0	V	5
Digital Output Characteristics	Logic 0 Voltage	I_O = 1 mA	0	—	0.5	V	5
	Logic 1 Voltage	I_O = −1 mA	4.5	—	5.0	V	5
Miscellaneous Characteristics	Power Dissipation	—	—	0.04	1.0	W	6
	SIGNAL IN Input Impedance	F = 1 kHz, paralleled with 15 pF	100k	—	—	ohms	
Power Requirements	Supply Current	VP − VND = 5 V ± 10% VP − VNA = 5 V ± 10%	—	8	18	mA	
	Power Supply Wide Band Noise (A = 0, B = 0)	VP − VND = 5 V VP − VNA = 5 V	—	—	10	mVpp	

Notes:

1. With a 5-volt power supply, an ambient temperature of 25° C, the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, −24 dBm equals 49 mVrms.)
2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.
3. With a 5-volt power supply, an ambient temperature of 25° C, the signal level at A + 5, the signal frequency deviation and twist at 0, and the signal applied 50 ms off and 50 ms on. The A level is the minimum detect level selected.
4. With the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The A level is the minimum detect level selected.
5. Logic levels are shown for a supply voltage (VP − VND) of 5 V, and are referenced to VND.
6. For a 5-volt power supply and an ambient temperature of 25° C.

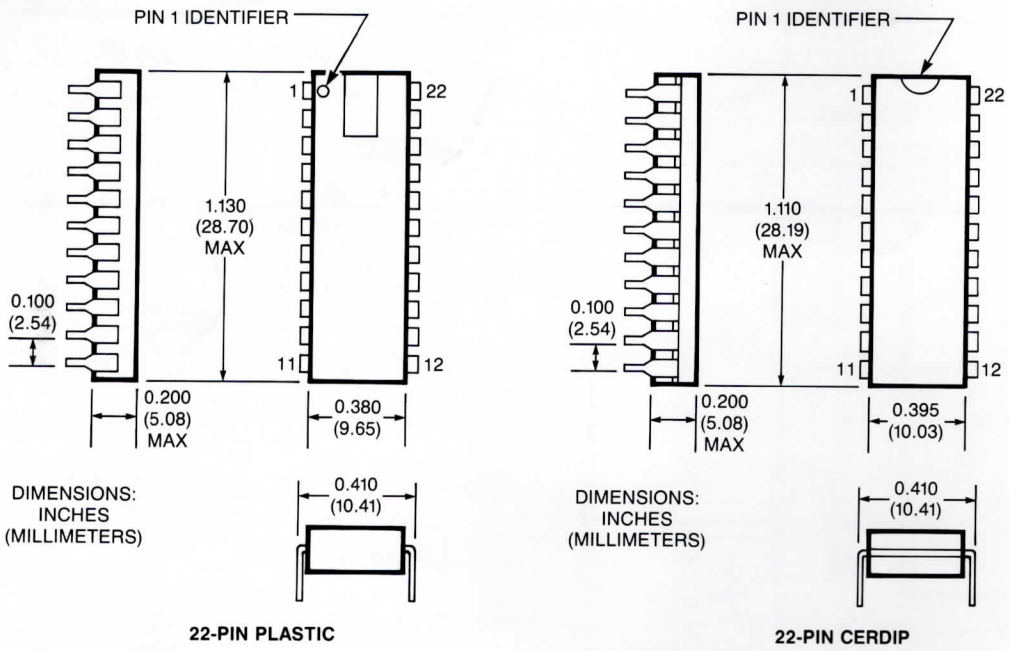

Figure 9 Package Dimensions

Teltone's experienced Field Service engineers are available for assistance in meeting your application needs:

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956-100 Issue 2 3/1/83